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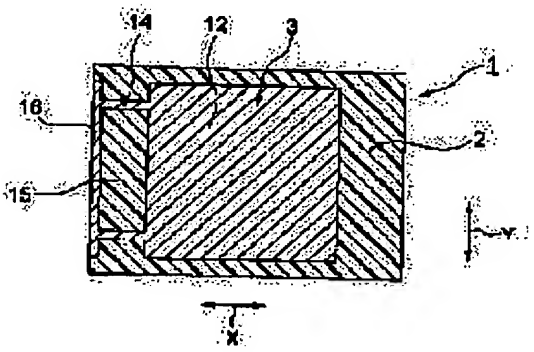
(54) LAYERED CERAMIC CAPACITOR AND ITS MANUFACTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a layered ceramic capacitor which can easily control ESR(equivalent series resistance) without changing most of the regular manufacturing processes of the layered ceramic capacitor and which is remarkably stable in a reliability test.
SOLUTION: The layered ceramic capacitor where an inner electrode layer 3 and a dielectric layer 2 are alternately laminated controls ESR by making the resistance of the leading part 14 of the inner electrode 3, which does not contribute to electrostatic capacity to be larger than that of an overlap part 12 contributed to electrostatic capacity. The lead part 14 has plural linear patterns. The obtained ESR of the layered ceramic capacitor can be controlled by controlling the number of linear patterns.



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CLAIMS

[Claim(s)]
[Claim 1] The stacked type ceramic condenser with which resistance of the drawer section of an internal electrode layer which does not participate in electrostatic capacity is characterized by having stronger resistance than resistance of the lap section which participates in electrostatic capacity in the stacked type ceramic condenser with which the laminating of an internal electrode layer and the dielectric layer was carried out by turns.
[Claim 2] The stacked type ceramic condenser according to claim 1 with which the cross sectional area of said drawer section is characterized by being smaller than the cross sectional area of said lap section.
[Claim 3] said drawer section -- a line -- the stacked type ceramic condenser according to claim 2 characterized by including a pattern.
[Claim 4] The stacked type ceramic condenser according to claim 2 with which thickness of said drawer section is characterized by being smaller than the thickness of said lap section.
[Claim 5] The manufacture approach of a stacked type ceramic condenser that resistance of the drawer section of an internal electrode layer which does not participate in electrostatic capacity is characterized by choosing the pattern configuration of the drawer section in the manufacture approach of a stacked type ceramic condenser of having the process which carries out the laminating of an internal electrode layer and the dielectric layer by turns so that it may have stronger resistance than resistance of the lap section which participates in electrostatic capacity in case the pattern of said internal electrode layer is formed on said dielectric layer.
[Claim 6] The manufacture approach of the stacked type ceramic condenser characterized by changing the pattern configuration of the drawer section of an internal electrode layer which does not participate in electrostatic capacity with the pattern configuration of the lap section which participates in electrostatic capacity in the manufacture approach of a stacked type ceramic condenser of having the process which carries out the laminating of an internal electrode layer and the dielectric layer by turns so that the equivalent series resistance of a stacked type ceramic condenser may serve as a predetermined value in case the pattern of said internal electrode layer is formed on said dielectric layer.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the stacked type ceramic condenser which can control equivalent series resistance (ESR) to accuracy, and its manufacture approach.
[0002]
[Description of the Prior Art] With development of an information communication link, the miniaturization of electronic equipment is progressing dramatically and especially the commercial scene of a cellular phone shows wonderful elongation. Although Regulator IC is built into these cellular phones, it has connected with this so that a stacked type ceramic condenser may constitute an output smoothing circuit.
[0003] However, equivalent series resistance (ESR) is dramatically low, the signal in a circuit carries out a loop formation, and an oscillation phenomenon arises, consequently a stacked type ceramic condenser tends to serve as a noise at the time of conversation. That is, in the secondary circuit of Regulator IC, if ESR of a smoothing circuit has big effect on the phase characteristic of a feedback loop and especially ESR becomes extremely low, a problem will be produced. That is, when the low stacked type ceramic condenser of ESR is used as a capacitor for smooth, a secondary smoothing circuit will consist of only L and a C component equivalent, and the phase component which exists in a circuit will become only **90 degrees and 0 degree, the allowances of a phase will be lost, and it will oscillate easily.
[0004] In order to control this oscillation, the big capacitor of ESR is needed. Although there is an electrolytic capacitor using a tantalum or aluminum as a big capacitor of ESR, since there is a decisive problem on dependability, such as a liquid spill, it cannot be used for a cellular phone. Therefore, the actual condition is that the noise at the time of the cellular-phone activity resulting from the capacitor for smoothing circuits is left.
[0005] In order to cancel such a trouble, the electronic parts which raised ESR of a stacked type ceramic condenser are proposed. For example, for patent No. 2578264, a metal oxide film is formed in the front face of the external terminal electrode of a stacked type ceramic condenser, and by operating this as resistance, ESR is raised and it is going to control resistance by the oxide-film thickness.
[0006] However, in case the capacitor indicated by the patent is manufactured actually, if control of oxidation of a terminal electrode is difficult and extent of oxidation is larger, an internal electrode will also oxidize, and it has a technical problem of it becoming impossible to achieve the function as a capacitor. Moreover, even if it can oxidize only a terminal electrode, since the terminal electrode has oxidized, inconvenience will arise.
[0007] That is, in case it plates on the front face of a terminal electrode, it is necessary to form a plating coat by electroless deposition, and in case it is the plating, it is necessary to cover with resin etc., since the terminal electrode has oxidized so that even a ceramic element assembly may not be plated. for this reason, the adhesive property between a process not only becoming complicated but the oxide film, and the plating film (nickel film) -- remarkable -- falling -- the meantime -- exfoliation -- being generated -- the need as electronic parts -- there is a fault that sufficient mechanical strength is not obtained. That is, when lead wire is prepared in the nickel-plating film of a terminal electrode, this lead wire will exfoliate easily.
[0008] Moreover, for example, what carried out the laminating of the resistive paste, such as ruthenium oxide, to the stacked type ceramic condenser, carried out simultaneous baking of this, and was made into the resistor is known as indicated by JP,59-225509,A. however, the case where a terminal electrode is prepared in this as it was -- an equal circuit -- C/R -- it cannot become a parallel circuit and or (LC/R) cannot obtain a series circuit. Moreover, in order to obtain a series circuit, the configuration of a terminal electrode will become complicated and a production process will also become complicated.

[0009] In addition, many of oxide resistors have many which have tempera dependence, and the equipment used in the environment where temperature conditions change is also expected the small device of temperature dependence. Furthermore, with the structure of the above-mentioned conventional capacitor, control of ESR is dramatically difficult and desired resistance cannot be acquired easily.
[0010] Recently, it is called for from various equipments including a power source or an electrical machinery and apparatus, and electronic equipment being used under various environments that there is no change of a property also under a severe service condition. It is important for especially ESR that passed and it is stable to the time.
[0011]
[Problem(s) to be Solved by the Invention] The object of this invention is offering the laminating ceramic condenser which could control ESR easily and was extremely stabilized also in the reliability trial, and the manufacture approach for which it was suitable in order to manufacture that capacitor, without completely changing the production process of the usual stacked type ceramic condenser.
[0012]
[Means for Solving the Problem] In order to attain the above-mentioned object, the stacked type ceramic condenser concerning this invention is characterized by having the resistance with stronger resistance of the drawer section of an internal electrode layer which does not participate in electrostatic capacity than resistance of the lap section which participates in electrostatic capacity in the stacked type ceramic condenser with which the laminating of an internal electrode layer and the dielectric layer was carried out by turns.
[0013] What is necessary is just to make the cross sectional area of said drawer section smaller than the cross sectional area of said lap section, in order to make resistance of said drawer section larger than resistance of the lap section.
[0014] said drawer section -- a line -- it is desirable that a pattern is included.
[0015] Thickness of said drawer section may be made smaller than the thickness of said lap section.
[0016] It is characterized by for the manufacture approach of the stacked type ceramic condenser concerning the 1st viewpoint of this invention to choose the pattern configuration of the drawer section in the manufacture approach of a stacked type ceramic condenser of having the process which carries out the laminating of an internal electrode layer and the dielectric layer by turns so that it may have resistance stronger in case the pattern of an internal electrode layer is formed on a dielectric layer than resistance of the lap section to which resistance of the drawer section of an internal electrode layer which does not participate in electrostatic capacity participates in electrostatic capacity.
[0017] In case the manufacture approach of the stacked type ceramic condenser concerning the 2nd viewpoint of this invention forms the pattern of an internal electrode layer on a dielectric layer, it is characterized by to change the pattern configuration of the drawer section of an internal electrode layer which does not participate in electrostatic capacity with the pattern configuration of the lap section which participates in electrostatic capacity in the manufacture approach of a stacked type ceramic condenser of having the process which carries out the laminating of an internal electrode layer and the dielectric layer by turns so that the equivalent series resistance of a stacked type ceramic condenser may serve as a predetermined value.
[0018]
[Function] In this invention, the stacked type ceramic condenser which can control ESR easily can be manufactured except changing the pattern of the drawer section in an internal electrode layer, without completely changing the production process of a stacked type ceramic condenser.
[0019] The configuration of the internal electrode layer of a stacked type ceramic condenser was seen from the flat-surface side, and has usually constituted the shape of a square. This is for enlarging area of the lap section with the internal electrode layer which counters through a dielectric layer, and acquiring electrostatic capacity to the maximum extent. Moreover, the drawer section of an internal electrode layer is only for securing connection with a terminal electrode, and does not contribute to electrostatic capacity at all.
[0020] ESR of a capacitor is controllable by lapping and changing the pattern configuration or thickness of this drawer section to the pattern configuration of the section with especially this invention. Therefore, in this invention, it becomes controllable [ESR], without completely reducing electrostatic capacity only by changing the configuration or thickness of the drawer section.
[0021]
[Embodiment of the Invention] Hereafter, this invention is explained based on the operation gestalt shown in a drawing. The sectional view of the stacked type ceramic condenser which drawing 1 requires for 1

operation gestalt of this invention, the sectional view which meets the II-II which shows drawing 2 to drawing 1 , the sectional view showing the pattern of the internal electrode layer which drawing 3 - drawing 5 require for other operation gestalten of this invention, the top view showing the pattern of the internal electrode layer which drawing 6 (A) requires for the pan of this invention at other operation gestalten, and drawing 6 (B) are important section sectional views which meet the VIB-VIB line of drawing 6 (A).

[0022] As shown in 1st operation gestalt drawing 1 , the stacked type ceramic condenser 1 concerning 1 operation gestalt of this invention has the capacitor element body 10 of a configuration of that the laminating of a dielectric layer 2 and the internal electrode layer 3 was carried out by turns. The external terminal electrode 4 of the internal electrode layer 3 arranged by turns inside the component body 10 and the couple through which it flows respectively is formed in the direction both ends of X of this capacitor element body 10. Although there is especially no limit in the configuration of the capacitor element body 10, it usually considers as the shape of a rectangular parallelepiped. Moreover, although what is necessary is for there to be especially no limit also in the dimension, and just to consider as a suitable dimension according to an application, it is usually x(0.6-5.6mm) (0.3-5.0mm) x (0.3-1.9mm) extent.

[0023] Each internal electrode layer 3 has the lap section 12 and the connection 16 which pulls out in the lap section 12 and is connected through the section 14, as shown in drawing 2 . The pattern of the internal electrode layer 3 and the right and left of the direction of X which show the pattern of the internal electrode layer 3 by which a laminating is carried out through a dielectric layer 2 to the bottom of the pattern of the internal electrode layer 3 shown in drawing 2 or a top to drawing 2 become reverse. And the connection 16 of the internal electrode layer 3 by which a laminating is carried out by turns through a dielectric layer 2 exposes to the front face of two edges where the capacitor element body 10 shown in drawing 1 counters by turns, and is connected to the external terminal electrode 4 of the couple arranged at those parts, respectively. Consequently, the internal electrode layer 3 by which the laminating was carried out through the dielectric layer 2 constitutes a capacitor circuit.

[0024] In each internal electrode layer 3, the lap section 12 is a part with which the internal electrode layer 3 by which a laminating is carried out by turns through a dielectric layer 2 sees and laps from a flat-surface view side, and the part participates in the electrostatic capacity of a capacitor. Moreover, the drawer section 14 and a connection 16 are parts with which the internal electrode layer 3 by which a laminating is carried out by turns through a dielectric layer 2 sees, and does not lap from a flat-surface view side, and are a part which does not participate in the electrostatic capacity of a capacitor but aims at connection with the external terminal electrode 4.

[0025] Since the lap section 12 is a part which participates in electrostatic capacity, in order to raise electrostatic capacity, it is desirable, and with this operation gestalt, that it is a large area as much as possible sees from a flat-surface view side, and it is a rectangle-like pattern. in order that a connection 16 may be a part directly connected to the external terminal electrode 4 shown in drawing 1 and may aim at positive connection -- the lap section 12 and abbreviation -- it is desirable to have the comparable direction width of face of Y.

[0026] the line to which resistance of the drawer section 14 of the internal electrode layer 3 which does not participate in electrostatic capacity is extended in the direction of X in the pattern of the drawer section 14 with this operation gestalt so that it may have stronger resistance than resistance of the lap section 12 which participates in electrostatic capacity as shown in drawing 2 -- it is considering as the pattern. the line which constitutes the drawer section 14 from this operation gestalt -- a pattern -- two -- carrying out -- two lines -- it lapped by the pattern and the section 12 and a connection 16 are connected electrically. two lines which constitute the drawer section 14 -- between patterns, a clearance 15 is formed and the dielectric layer 2 of the direction of a laminating is continuing in the clearance 15. the line which constitutes the drawer section 14 -- although especially the line breadth of a pattern is not limited, it is min, and it is comparable as the thickness of the internal electrode layer 3, is max, and is 1/2 of the width of face of the lap section 12.

[0027] Next, the manufacture approach of the stacked type ceramic condenser 1 of this operation gestalt is shown in a detail.

The paste for [paste for dielectric layers] dielectric layers kneads a dielectric raw material and an organic vehicle, and is manufactured. The powder according to the presentation of a dielectric layer is used for a dielectric raw material. Although it is not limited especially as dielectric materials and various dielectric materials may be used, titanium oxide, titanium system multiple oxides, or such mixture are desirable, for example. as a titanium oxide system -- the need -- responding -- NiO, CuO, and Mn3 O4 aluminum2 O3 MgO and SiO2 etc. -- a total of 0.001 -- about -30wt% -- added TiO2 A system is mentioned. moreover -- as a titanic-acid system multiple oxide -- barium titanate BaTiO3 etc. -- it is mentioned. the atomic ratio of

Ba/Ti -- 0.95 to about 1.20 -- good -- BaTiO3 **** -- MgO, CaO, Mn3 O4 [redacted] O3 V2 O5 ZnO and ZrO2 Nb2 O5 Cr2 O3 Fe 2O3 P2 O5 Na2 O and K2 O etc. -- a total of 0.001 -- about -30wt% -- it may be added. Moreover, it is SiO(Ba, calcium) 2 because of adjustment of burning temperature and coefficient of linear expansion. Glass, such as glass, may be added.

[0028] Especially the manufacture approach of a dielectric raw material is BaTiO3 which carried out hydrothermal synthesis when it was not limited, for example, barium titanate was used. The approach of mixing an accessory constituent raw material can be used. Moreover, BaCO3 TiO2 The dry type synthesis method to which temporary quenching of the mixture with an accessory constituent raw material is carried out, and it carries out solid phase reaction may be used. Moreover, temporary quenching of the mixture of the precipitate and the accessory constituent raw material which were obtained with the coprecipitation method, the sol-gel method, the alkali hydrolyzing method, the precipitate mixing method, etc. may be carried out, and it may be compounded. In addition, an oxide, the various compounds which turn into an oxide by baking, for example, a carbonate, an oxalate, a hydroxide, an organometallic compound, etc. can use more than a kind for an accessory constituent at least. Although what is necessary is just to determine the mean particle diameter of dielectric materials according to the diameter of average crystal grain of the dielectric layer made into the object, powder with a mean particle diameter of about 0.3-1.0 micrometers is usually used for it. A dielectric paste kneads a dielectric raw material and an organic vehicle is manufactured in it.

[0029] An organic vehicle dissolves a binder into an organic solvent. What is necessary is not to limit especially the binder used for an organic vehicle, but just to choose it from the various usual binders, such as ethyl cellulose, suitably. Moreover, what is necessary is not to limit especially the organic solvent to be used, either but just to choose from various organic solvents, such as terpineol, butyl carbitol, an acetone, and toluene, suitably according to print processes, the sheet method, and the approach of using.

[0030] Although especially the thickness of a dielectric layer that is a hit much more is not limited, it is usually about 1.5-20 micrometers. Moreover, the number of laminatings of a dielectric layer is usually 100 to about 300.

[0031] Although especially the electric conduction material of the paste for [paste for internal electrode layers] internal electrode layers is not limited, the thing which is chosen from nickel and Cu and which consist more than of a kind at least is desirable. Moreover, a cheap base metal can be used by using what has reducibility-proof for a dielectric lamination ingredient. For this reason, especially as electric conduction material, nickel or nickel alloy is desirable. As a nickel alloy, the element more than a kind chosen from Mn, Cr, Co, aluminum, etc. and the alloy of nickel are desirable, and, as for nickel content in an alloy, it is desirable that it is more than 95wt%. in addition -- the inside of nickel or nickel alloy -- various minor constituents, such as P, -- or less about 0.1wt% -- it may be contained.

[0032] The paste for internal electrodes kneads and adjusts the various above-mentioned conductive metals, an alloy or the various oxide used as the electric conduction material described above after baking, an organometallic compound, resinate, etc. and the above-mentioned organic vehicle. Although what is necessary is just to determine the thickness of the internal electrode layer 3 suitably according to an application, it is desirable that it is about 0.5-5 micrometers.

[0033] The paste for [paste for external terminal electrodes] external terminal electrodes contains electric conduction material, a glass frit, and an organic vehicle. Although said electric conduction material is chosen from Ag, Au, Pt, Pd, Cu, and nickel by more than kind at least, since it is cheap, Cu, nickel, or these alloys are desirable, and especially its Cu is desirable. A glass frit is added in order to secure adhesion with sintering acid or a chip element assembly to these electric conduction material.

[0034] Mean particle diameter of electric conduction material is set to 0.01-10 micrometers. Condensation of an electric conduction material particle becomes intense, and when particle size is smaller than this, it can be burned, and it becomes easy to produce a crack in a terminal electrode, and the time of spreading of the paste for terminal electrodes, and desiccation, or when particle size is larger than this, pasting sometimes becomes difficult. Moreover, mean particle diameter of a glass frit is set to 0.01-30 micrometers. If particle size is smaller than this, sintering of electric conduction material will become uneven, it becomes the cause of making a terminal electrode generating a crack, and if larger than this, distribution of glass will worsen, and it is in the inclination for the adhesive property of a terminal electrode and an element assembly to fall. These electric conduction material and a glass frit are distributed in a vehicle, and the paste for terminal electrodes is obtained.

[0035] Especially a glass frit presentation is not limited. However, when Cu is used for electric conduction material, it is required to be what achieves the function as glass also on the need of calcinating a terminal

electrode, and under these ambient atmospheres at neutrality or a reducing atmosphere. As such a thing, for example Silicic-acid glass (SiO2 : 20 - 80wt%, Na 2 O:80 - 20wt%), Borosilicate glass (B-2 O3 : 5 - 50wt% and SiO2 :5 - 70wt% and PbO:1 - 10wt% and K2 O:1 - 15wt%), A kind of the glass frit chosen from alumina silicic-acid glass (aluminum2 O3 : 1 - 30wt% and SiO2 :10 - 60wt%, Na 2 O:5 - 15wt% and CaO:1 - 20wt% and B-2 O3 :5 - 30wt%), or two sorts or more What is necessary is just to use. this -- the need -- responding -- CaO: -- 0.01 - 50wt% and BaO:0.01 - 50wt% and MgO:0.01 - 5wt% and -ZnO:0.01 - 70wt% and PbO:0.01 - 5wt% and Na2 O:0.01 - 10wt% and K2 O:0.01 - 10wt% and MnO2 : What is necessary is to mix and just to use additives, such as 0.01 - 20wt%, so that it may become a predetermined presentation. Although especially the content of the glass to the metal component which is electric conduction material is not limited, it is usually about 0.5-15wt% to a metal component. What is necessary is just to use an above-mentioned thing as an organic vehicle.

[0036] What is necessary is for there to be especially no limit in the content of the organic vehicle under each paste which carried out the [content of organic vehicle] above, and to make the usual content, for example, a binder, into about 1-5wt%, and just to make a solvent into 10 - 50wt%. Moreover, during each paste, the additive chosen from various dispersants, a plasticizer, a dielectric, an insulator, etc. if needed may contain. As for these total contents, considering as less than [10wt%] is desirable.

[0037] When using [production of Green chip] print processes, the paste for dielectrics and the paste for internal electrodes are printed in the shape of [, such as PET,] a substrate. A laminating is carried out so that one side of the edge of the paste for internal electrodes may be outside exposed by turns from the edge of a dielectric paste at this time. Then, thermocompression bonding is carried out, and after cutting and chip-izing in a predetermined configuration, it exfoliates from a substrate and considers as the Green chip.

[0038] Moreover, when using the sheet method, a green sheet is formed using the paste for dielectric layers, the paste for internal electrode layers is printed on this green sheet, these are repeated by turns and carry out a laminating, and it cuts in a predetermined configuration and considers as the Green chip.

[0039] With this operation gestalt, as it is shown in drawing 2 in case the paste for internal electrodes is printed for example, the pattern for internal electrodes which consists of the lap section 12, the drawer section 14, and a connection 16 is formed.

[0040] Although they may be the usual thing, when using base metal, such as nickel and nickel alloy, for the electric conduction material of an internal electrode layer, as for the conditions of the debinder processing performed before [debinder process] baking, it is desirable to carry out on condition that the following especially.

Especially an hour 5-300 degrees C /Programming rate : A 10-100 degree-C/hour retention temperature:200-400 degree-C/hour, Especially for 0.5 to 24 hours Especially, 250-300-degree-C [/] hour temperature holding time : the ambient atmosphere at the time of baking of the [baking process] Green chip in 5 - 20-hour ambient atmosphere:air Although what is necessary is just to choose suitably according to the class of electric conduction material of the paste for internal electrodes A firing environments is N2 when using base metal, such as nickel and nickel alloy, as electric conduction material. It considers as a principal component and is H2. H2 obtained with the water vapor pressure in 10-35 degrees C 1 to 10% What mixed O gas is desirable. Oxygen tension is 10-8 to 10-12. Considering as an atmospheric pressure is desirable. When oxygen tension is said under range, a lifting and breaking off have the electric conduction material of an internal electrode in abnormality sintering. Moreover, when oxygen tension crosses said range, it is in the inclination for an internal electrode to oxidize. As for especially the retention temperature at the time of baking, it is desirable to consider as 1200-1300 degrees C 1100-1400 degrees C. An internal electrode will become easy to break off, if eburnation is inadequate in retention temperature being said under range and said range is crossed. Moreover, especially the temperature holding time at the time of baking has 1 - 3 desirable hours for 0.5 to 8 hours.

[0041] When it calcinates by [annealing process] reducing atmosphere, it is desirable to give annealing to a laminating chip capacitor. Annealing is processing for reoxidating a dielectric layer, and, thereby, can lengthen accelerated aging of insulation resistance remarkable.

[0042] As for especially the oxygen tension of an annealing ambient atmosphere, it is desirable to consider as 10-6 - 10-8 atmospheric pressure ten to six or more atmospheric pressures. If reoxidation of a dielectric layer is difficult in oxygen tension being said under range and said range is crossed, an internal electrode will oxidize.

[0043] As for especially the retention temperature of annealing, it is desirable to consider as 500-1000 degrees C 1100 degrees C or less. If the inclination it to become being said under range oxidizing [of a dielectric layer] retention temperature inadequate, and for accelerated aging of insulation resistance to

become short is shown and said range is crossed, an internal electrode will [redacted]ize, not only capacity falls, but it reacts with a dielectric base and accelerated aging becomes short. In addition, an annealing process may consist of only temperature up and a temperature fall. In this case, it is not necessary to take the temperature holding time, and retention temperature is synonymous with a maximum temperature. Moreover, especially the temperature holding time has 2 - 10 desirable hours for 0 to 20 hours. In a controlled atmosphere, it is N2. H2 humidified It is desirable to use gas.

[0044] In addition, it sets at each process of the above-mentioned debinder processing, baking, and annealing, and is N2. H2 What is necessary is just to use UETTA etc., in order to humidify mixed gas etc. The water temperature in this case has desirable about 5-75 degrees C. Debinder down stream processing, a baking process, and an annealing process may be performed continuously, or may be performed independently. When performing these continuously, after debinder processing, it may not cool, but an ambient atmosphere may be changed and performed independently. When these are performed continuously, the ambient atmosphere was changed, and it calcinates by having carried out temperature up to the retention temperature of baking continuously, it subsequently cools [it did not cool, but] after debinder processing and the retention temperature in an annealing process is reached, it is desirable to change an ambient atmosphere and to perform annealing.

[0045] Moreover, when performing these independently, debinder down stream processing is lowered to a room temperature, after carrying out temperature up and carrying out predetermined time maintenance to predetermined retention temperature. Let the debinder ambient atmosphere in that case be the same thing as the case where it carries out continuously. Moreover, a debinder process and a baking process are performed continuously, and it may be made to perform only an annealing process independently, and only a debinder process is performed independently and it may be made to perform a baking process and an annealing process continuously.

[0046] The paste for [terminal electrode formation] terminal electrodes is applied to a sintered compact chip. What is necessary is to just be based on a dip method etc., although not limited especially as a spreading process. Although what is necessary is for the sintered compact chip size which it is not limited and is applied just to adjust especially the coverage of the paste for terminal electrodes suitably, it is usually about 5-100 micrometers. It dries after applying the paste for terminal electrodes. It is desirable to perform desiccation at about 60-150 degrees C for 10 minutes to about 1 hour.

[0047] After applying the paste for terminal electrodes as mentioned above and drying, baking to a chip element assembly is performed. Baking conditions are N2. Neutral atmosphere, or N2 and H2 It is desirable to carry out by holding at 600 degrees C - 1000 degrees C in reducing atmosphere, such as mixed gas, for about 0 to 1 hour.

[0048] nickel layer, Sn layer, or a Sn-Pb alloy layer is formed with electrolysis plating on the above-mentioned terminal electrode if needed [[deposit]]. Although especially the thickness of a deposit is not limited, it is usually about 0.1-10 micrometers.

[0049] With a [operation of stacked type ceramic condenser and its manufacture approach] book operation gestalt, the stacked type ceramic condenser 1 which can control ESR easily can be manufactured except changing the pattern of the drawer section 14 in the internal electrode layer 3, without completely changing the production process of a stacked type ceramic condenser.

[0050] ESR of a capacitor is controllable by lapping and changing the pattern configuration of this drawer section 14 to the pattern configuration of the section 12 with especially this operation gestalt. Therefore, with this operation gestalt, it becomes controllable [ESR], without completely reducing electrostatic capacity only by changing the configuration of the drawer section 14.

[0051] Although especially the concrete value of ESR is not limited, it is 0.5ohms - about 10ohms, and are usually 0.5-5ohm preferably. The stacked type ceramic condenser which has ESR of this range can demonstrate engine performance sufficient as a capacitor for Regulators IC.

[0052] As shown in 2nd operation gestalt drawing 3 , the pattern configuration of lap section 12of internal electrode layer 3a by which laminating is carried out through dielectric layer 2 a, and connection 16a presupposes that it is the same as that of the thing of the operation gestalt shown in drawing 2 , and is made different from the thing of the operation gestalt which shows only the pattern configuration of drawer section 14a to drawing 2 in stacked type ceramic condenser 1a concerning this operation gestalt.

[0053] namely, four lines extended in the direction of X in drawer section 14a with this operation gestalt -- a pattern -- constituting -- **** -- these lines -- it lapped with the pattern and section 12a and connection 16a are connected. the line which constitutes drawer section 14a -- ESR of the stacked type ceramic condenser obtained eventually is controllable by controlling the number of a pattern. a line -- resistance of drawer

section 14a falls, so that the number of a pattern increases. The same operation as the stacked type ceramic condenser 1 which stacked type ceramic condenser 1a concerning this operation gestalt also requires for said 1st operation gestalt is done so.

[0054] As shown in 3rd operation gestalt drawing 4 , the pattern configuration of lap section 12of internal electrode layer 3b by which laminating is carried out through dielectric layer 2 b, and connection 16b presupposes that it is the same as that of the thing of the operation gestalt shown in drawing 2 , and is made different from the thing of the operation gestalt which shows only the pattern configuration of drawer section 14b to drawing 2 in stacked type ceramic condenser 1b concerning this operation gestalt.

[0055] namely, five lines extended in the direction of X in drawer section 14b with this operation gestalt -- the line extended in the direction of Y so that these mid-position may be connected to a pattern -- pattern 18b -- constituting -- **** -- these lines -- it lapped with the pattern and section 12b and connection 16b are connected. the line which constitutes drawer section 14b -- ESR of the stacked type ceramic condenser obtained eventually is controllable by controlling the number of a pattern. a line -- resistance of drawer section 14b falls, so that the number of a pattern increases. The same operation as the stacked type ceramic condenser 1 which stacked type ceramic condenser 1b concerning this operation gestalt also requires for said 1st operation gestalt is done so.

[0056] As shown in 4th operation gestalt drawing 5 , by stacked type ceramic condenser 1c concerning this operation gestalt, the pattern configuration of lap section 12c of internal electrode layer 3c by which a laminating is carried out through a dielectric layer 2 presupposes that it is the same as that of the thing of the operation gestalt shown in drawing 2 , and it has enlarged the direction width of face of X of connection 16c while making the pattern configuration of drawer section 14c different from the thing of the operation gestalt shown in drawing 2 .

[0057] five lines extended in the direction of X in drawer section 14c with this operation gestalt -- a pattern -- constituting -- **** -- these lines -- it lapped with the pattern and section 12c and connection 16c are connected. the line which constitutes drawer section 14c -- ESR of the stacked type ceramic condenser obtained eventually is controllable by controlling the number of a pattern. a line -- resistance of drawer section 14c falls, so that the number of a pattern increases. The same operation as the stacked type ceramic condenser 1 which stacked type ceramic condenser 1c concerning this operation gestalt also requires for said 1st operation gestalt is done so.

[0058] As shown in 5th operation gestalt drawing 6 (A) and (B), although the flat-surface view pattern configuration of 12d of lap sections of 3d of internal electrode layers by which a laminating is carried out through a dielectric layer 2, 14d of drawer sections, and 16d of connections is the same as that of the conventional thing, by 1d of stacked type ceramic condensers concerning this operation gestalt, the point which has made thin thickness of 14d of drawer sections compared with the thickness of 12d of lap sections differs from the former.

[0059] That is, with this operation gestalt, thickness of 14d of drawer sections is made thin compared with the thickness of 12d of lap sections, and 16d of connections. Resistance of the part can be raised by making thin thickness of 14d of drawer sections. Moreover, ESR of the stacked type ceramic condenser obtained eventually is controllable by controlling the thickness of 14d of drawer sections. Resistance of 14d of drawer sections increases, so that the thickness of 14d of drawer sections becomes thin. The same operation as the stacked type ceramic condenser 1 which even 1d even of stacked type ceramic condensers concerning this operation gestalt requires for said 1st operation gestalt is done so.

[0060] it is not limited to the operation [which are other operation gestalten] gestalt which mentioned this invention above, and within the limits of this invention, many things can be boiled and it can change. For example, the pattern which changes a drawer sections [14, 14a-14d] configuration is not limited to the operation gestalt mentioned above, and no matter the pattern of the drawer section may be a spiral pattern, or it may be a wavelike pattern and may be what other pattern configurations, it is not cared about.

[0061] Furthermore, in this invention, the same operation effectiveness is acquired also by constituting the drawer sections 14, 14a-14d of an internal electrode layer from the lap sections 12, 12a-12d by the high electric conduction material of resistance.

[0062]

[Example] Hereafter, although this invention is explained based on a still more detailed example, this invention is not limited to these examples.

[0063] It is $BaCO_3$ as a main raw material of example 1 dielectric layer. (mean particle diameter: 2.0 micrometers) And TiO_2 (mean particle diameter: 2.0 micrometers) It prepared. The atomic ratio of Ba/Ti is 1.00. moreover -- in addition, $BaTiO_3$ receiving -- as an additive -- $MnCO_3$ 0.2wt(s)% and $MgCO_3$ 0.2wt

(s)% and Y2 O3 2.1wt(s)% and CaO (Ba, calcium)3 2.2wt(s)% -- it prepared. Each raw material powder was mixed with the underwater ball mill, and it dried. Temporary quenching of the obtained mixed powder was carried out at 1250 degrees C for 2 hours. The underwater ball mill ground this temporary-quenching powder, and it dried. The methylene chloride and the acetone were added to the obtained temporary-quenching powder as acrylic resin and an organic solvent as an organic binder, and it mixed further, and considered as the dielectric slurry. The obtained dielectric slurry was used as the dielectric green sheet with the doctor blade method.

[0064] nickel powder (mean diameter: 0.8 micrometers) was prepared as an internal electrode layer ingredient, terpineol was added to this as ethyl cellulose and an organic solvent as an organic binder, and it kneaded using 3 rolls, and considered as the internal electrode paste.

[0065] as the electrical conducting material of an external terminal electrode -- Cu powder (mean diameter: 0.5 micrometers) and Cu powder -- receiving -- a strontium system glass frit -- 7wt(s)% -- it added, terpineol was added to this as acrylic resin and an organic solvent as an organic binder, and it kneaded using 3 rolls, and considered as the paste for the 1st metal layers.

[0066] In order to obtain predetermined thickness, several sheet laminating of the dielectric green sheet was carried out, the 200-sheet laminating of the green sheet printed so that the edge of the paste for internal electrodes might be outside exposed from the edge of the green sheet for dielectric layers by turns with screen printing using the internal electrode pattern shown in drawing 2 on it was carried out, and it carried out thermocompression bonding. Subsequently, it cut so that the chip configuration after baking might become the vertical 2.0x width 1.2x thickness of 1.2mm, and the Green chip was obtained.

[0067] N2 which humidified the obtained Green chip +H2 (H2:3%) H2 which held for 3 hours, calcinated at 1300 degrees C among the ambient atmosphere, and was humidified further It held at 1000 degrees C in the ambient atmosphere of ten to oxygen tension 7 atmospheric pressure for 2 hours, and the chip sintered compact was obtained. The above-mentioned paste for terminal electrodes is applied to the both ends of the obtained sintered compact, and it dries after that, and is N2-H2. It heat-treated by having held for 10 minutes at 770 degrees C among the ambient atmosphere, and the terminal electrode was obtained.

[0068] Then, the plating film was formed with electrolysis plating in order of nickel and Sn on this terminal electrode. The electrostatic capacity of the obtained stacked type ceramic condenser sample was 2.0 micro F.

[0069] The electrostatic capacity of a stacked type ceramic condenser and the value of ESR which carried out the laminating of the internal electrode structure shown in drawing 1 , and produced it are shown in a table 1. The measured number is 50 pieces and shows the average. ESR was measured with the LCR meter.

[0070]

[A table 1]

内部電極パターンと電気特性

	静電容量（μF）	ESR（Ω）
実施例1	2．0	2．44
実施例2	2．0	1．10
実施例3	2．0	0．92
実施例4	2．0	0．68
比較例1	2．0	0．0005

[0071] Moreover, when it was made to operate by 100kHz, using the stacked type ceramic condenser of this example 1 as a capacitor for smooth of Regulator IC, it operated normally, without producing voltage variation, such as an oscillation.

[0072] Moreover, change was not accepted in fluctuation of ESR, and other electrical properties (electrostatic capacity, insulation resistance) by the elevated-temperature load test (85 degrees C, twice as many electrical-potential-difference impression as rating, 1000 hours) and anti-humidity load test (85 degrees C, 85%, rated voltage impression, 1000 hours) which are an accelerated test of a capacitor.
[0073] Except having considered as the pattern shown in drawing 3 as a pattern of an example 2 internal-electrode layer, like said example 1, the stacked type ceramic condenser sample was produced and electrostatic capacity and the value of ESR were calculated. A result is shown in a table 1.
[0074] Moreover, when it was made to operate by 100kHz, using the stacked type ceramic condenser of this example 2 as a capacitor for smooth of Regulator IC, it operated normally, without producing voltage variation, such as an oscillation.
[0075] Moreover, change was not accepted in fluctuation of ESR, and other electrical properties (electrostatic capacity, insulation resistance) by the elevated-temperature load test and anti-humidity load test which are an accelerated test of a capacitor.
[0076] Except having considered as the pattern shown in drawing 4 as a pattern of an example 3 internal-electrode layer, like said example 1, the stacked type ceramic condenser sample was produced and electrostatic capacity and the value of ESR were calculated. A result is shown in a table 1.
[0077] Moreover, when it was made to operate by 100kHz, using the stacked type ceramic condenser of this example 3 as a capacitor for smooth of Regulator IC, it operated normally, without producing voltage variation, such as an oscillation.
[0078] Moreover, change was not accepted in fluctuation of ESR, and other electrical properties (electrostatic capacity, insulation resistance) by the elevated-temperature load test and anti-humidity load test which are an accelerated test of a capacitor.
[0079] Except having considered as the pattern shown in drawing 5 as a pattern of an example 4 internal-electrode layer, like said example 1, the stacked type ceramic condenser sample was produced and electrostatic capacity and the value of ESR were calculated. A result is shown in a table 1.
[0080] Moreover, when it was made to operate by 100kHz, using the stacked type ceramic condenser of this example 4 as a capacitor for smooth of Regulator IC, it operated normally, without producing voltage variation, such as an oscillation.
[0081] Moreover, change was not accepted in fluctuation of ESR, and other electrical properties (electrostatic capacity, insulation resistance) by the elevated-temperature load test and anti-humidity load test which are an accelerated test of a capacitor.
[0082] Except having considered as the pattern of the conventional example with which the pattern of the lap section, the drawer section, and a connection sees from a flat-surface view side, and becomes rectangle-like in one altogether as a pattern of an example of comparison 1 internal-electrode layer, like said example 1, the stacked type ceramic condenser sample was produced and electrostatic capacity and the value of ESR were calculated. A result is shown in a table 1.
[0083] Moreover, when it was made to operate by 100kHz, using the stacked type ceramic condenser of the example 1 of a comparison as a capacitor for smooth of Regulator IC, voltage variation, such as an oscillation, was observed.
[0084] Moreover, fluctuation of ESR was observed in the elevated-temperature load test and anti-humidity load test which are an accelerated test of a capacitor.
[0085] By changing the configuration of the drawer section of an internal electrode, i.e., the cross section, (or volume) shows that ESR is controllable so that clearly from the assessment table 1.
[0086]
[Effect of the Invention] As explained above, according to this invention, by selecting the configuration of the drawer section of an internal electrode, it becomes controllable [ESR] easily and the stacked type ceramic condenser possessing desired ESR is obtained only by changing the pattern at the time of forming an internal electrode, without hardly changing the process of the usual stacked type ceramic condenser.

[Translation done.]

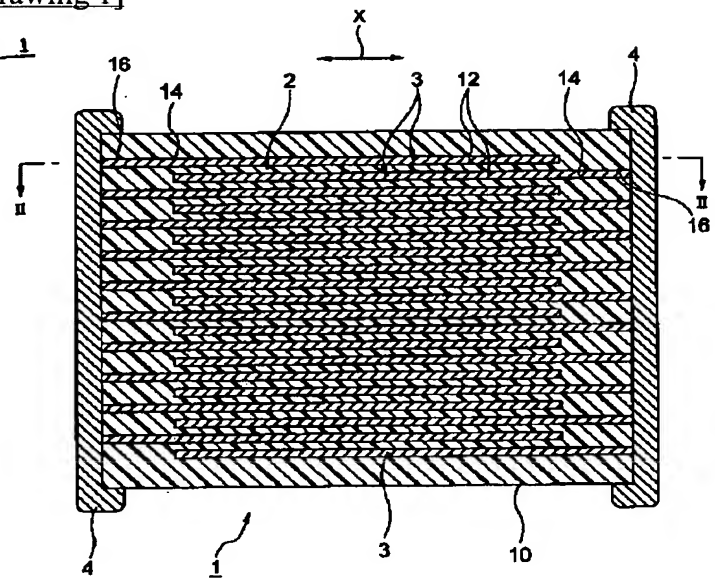
* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

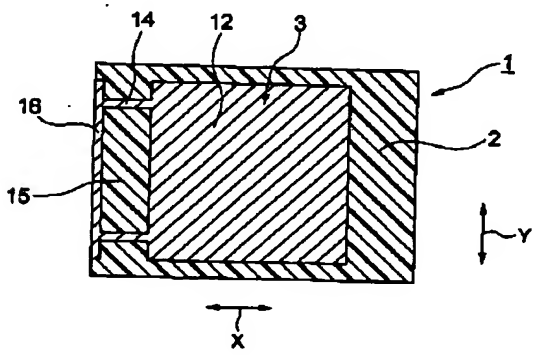
[Drawing 1]

図 1



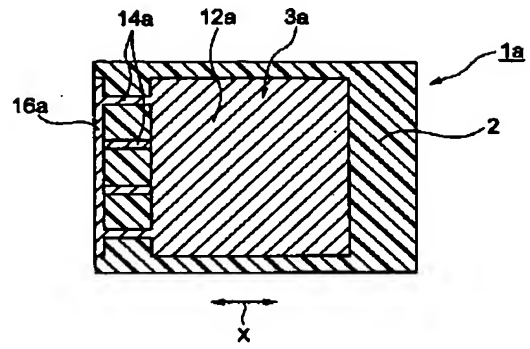
[Drawing 2]

図 2



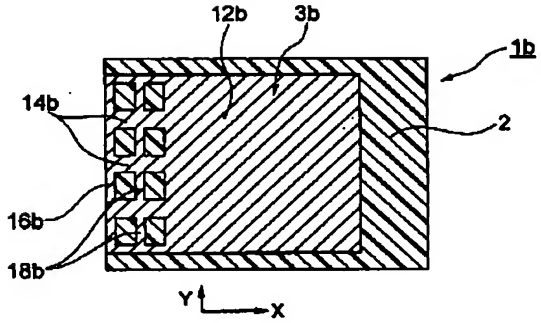
[Drawing 3]

図 3



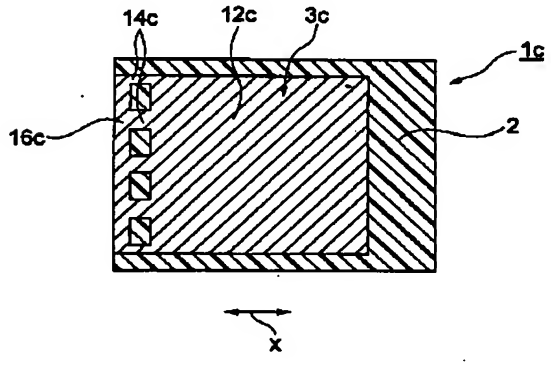
[Drawing 4]

図 4



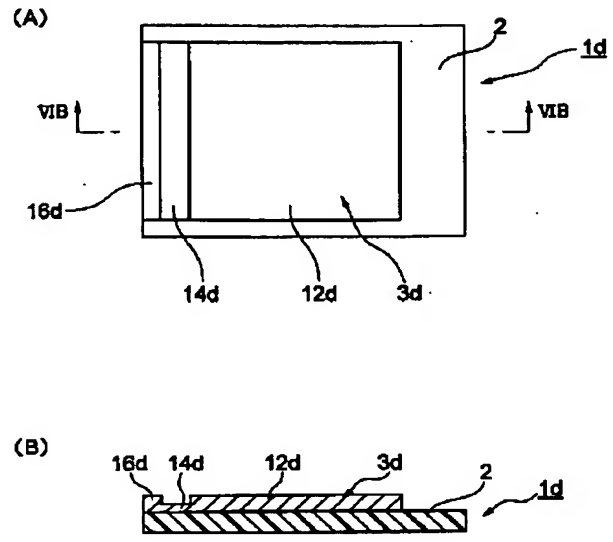
[Drawing 5]

図 5



[Drawing 6]

図 6



[Translation done.]

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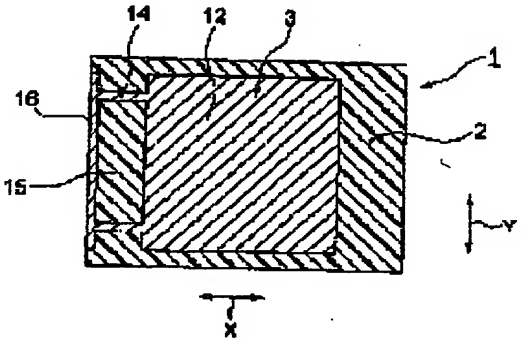
(71)Applicant : TDK CORP
(72)Inventor : IGARASHI KATSUHIKO

(54) LAYERED CERAMIC CAPACITOR AND ITS MANUFACTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a layered ceramic capacitor which can easily control ESR(equivalent series resistance) without changing most of the regular manufacturing processes of the layered ceramic capacitor and which is remarkably stable in a reliability test.
SOLUTION: The layered ceramic capacitor where an inner electrode layer 3 and a dielectric layer 2 are alternately laminated controls ESR by making the resistance of the leading part 14 of the inner electrode 3, which does not contribute to electrostatic capacity to be larger than that of an overlap part 12 contributed to electrostatic capacity. The lead part 14 has plural linear patterns. The obtained ESR of the layered ceramic capacitor can be controlled by controlling the number of linear patterns.



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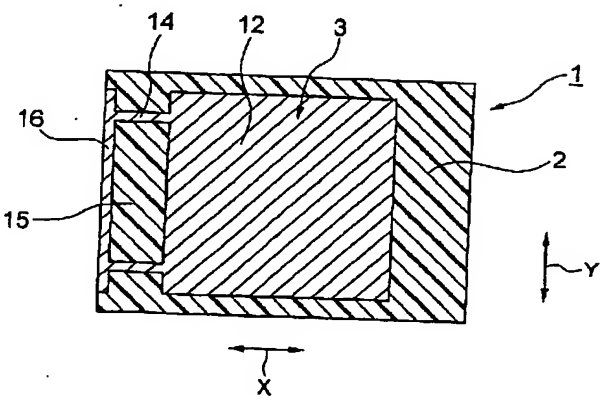
最終頁に続く

(54)【発明の名称】　積層セラミックコンデンサおよび積層セラミックコンデンサの製造方法

(57)【要約】
【課題】　通常の積層セラミックコンデンサの製造工程をほとんど変えることなく、容易にＥＳＲ（等価直列抵抗）を制御でき、かつ信頼性試験においても極めて安定した積層セラミックコンデンサを提供することである。
【解決手段】　内部電極層３と誘電体層２とを交互に積層した積層セラミックコンデンサにおいて、静電容量に関与しない内部電極３の引き出し部１４の抵抗を静電容量に関与する重なり部１２の抵抗より大きくすることによりＥＳＲを制御する。引き出し部１４は、たとえば複数の線状パターンである。線状パターンの数を制御することなどで、得られる積層セラミックコンデンサのＥＳＲを制御することができる。

図　2



【特許請求の範囲】
【請求項１】　内部電極層と誘電体層とが交互に積層された積層セラミックコンデンサにおいて、
静電容量に関与しない内部電極層の引き出し部の抵抗が、静電容量に関与する重なり部の抵抗より大きな抵抗を有することを特徴とする積層セラミックコンデンサ。
【請求項２】　前記引き出し部の横断面積が、前記重なり部の横断面積よりも小さいことを特徴とする請求項１に記載の積層セラミックコンデンサ。
【請求項３】　前記引き出し部が、線状パターンを含むことを特徴とする請求項２に記載の積層セラミックコンデンサ。
【請求項４】　前記引き出し部の厚みが、前記重なり部の厚みよりも小さいことを特徴とする請求項２に記載の積層セラミックコンデンサ。
【請求項５】　内部電極層と誘電体層とを交互に積層する工程を有する積層セラミックコンデンサの製造方法において、
前記誘電体層の上に前記内部電極層のパターンを形成する際に、静電容量に関与しない内部電極層の引き出し部の抵抗が、静電容量に関与する重なり部の抵抗より大きな抵抗を有するように、引き出し部のパターン形状を選択することを特徴とする積層セラミックコンデンサの製造方法。
【請求項６】　内部電極層と誘電体層とを交互に積層する工程を有する積層セラミックコンデンサの製造方法において、
前記誘電体層の上に前記内部電極層のパターンを形成する際に、積層セラミックコンデンサの等価直列抵抗が所定の値となるように、静電容量に関与しない内部電極層の引き出し部のパターン形状を、静電容量に関与する重なり部のパターン形状と異ならせることを特徴とする積層セラミックコンデンサの製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、等価直列抵抗（ＥＳＲ）を正確に制御し得る積層セラミックコンデンサおよびその製造方法に関する。
【０００２】
【従来の技術】情報通信の発達にともない、電子機器の小型化が非常に進んでおり、特に携帯電話の市場は驚異的な伸びを示している。これら携帯電話には、レギュレータＩＣが組み込まれているが、これには積層セラミックコンデンサが出力平滑化回路を構成するように接続してある。
【０００３】しかしながら、積層セラミックコンデンサは、等価直列抵抗（ＥＳＲ）が非常に低く、回路内の信号がループし発振現象が生じ、その結果、会話時の雑音となり易い。つまり、レギュレータＩＣの二次側回路では、平滑回路のＥＳＲが帰還ループの位相特性に大きな影響を与え、特にＥＳＲが極端に低くなると問題を生じる。すなわち、平滑用コンデンサとしてＥＳＲの低い積層セラミックコンデンサを使用した場合、二次側平滑回路が等価的にＬとＣ成分のみで構成されてしまい、回路内に存在する位相成分が±９０°および０°のみとなり、位相の余裕がなくなって容易に発振してしまう。
【０００４】この発振を抑制するためには、ＥＳＲの大きなコンデンサが必要となる。ＥＳＲの大きなコンデンサとしては、タンタルあるいはアルミニウムを用いた電解コンデンサがあるが、液漏れ等の信頼性上の決定的な問題があるために、携帯電話には使用できない。そのため、平滑化回路用コンデンサに起因する携帯電話使用時の雑音は放置されたままであるのが現状である。
【０００５】このような問題点を解消するために、積層セラミックコンデンサのＥＳＲを高めた電子部品が提案されている。例えば、特許第２５７８２６４号には、積層セラミックコンデンサの外部端子電極の表面に金属酸化膜を形成し、これを抵抗として機能させることによりＥＳＲを高めており、その酸化膜厚で抵抗値を制御しようとしている。
【０００６】しかしながら、その特許に開示されたコンデンサを実際に製造する際に、端子電極の酸化の制御が難しく、酸化の程度が少しでも大きいと内部電極も酸化されてしまい、コンデンサとしての機能を果たすことができなくなってしまうという課題を有する。また、仮に端子電極のみを酸化することができても、端子電極が酸化されているために不都合が生じる。
【０００７】すなわち、端子電極が酸化されているために、端子電極の表面にメッキを行う際に、無電解メッキでメッキ皮膜を形成する必要があり、そのメッキの際にセラミック素体までもがメッキされないように樹脂等で被覆する必要がある。このため、工程が複雑になるばかりでなく、酸化物膜とメッキ膜（Ｎｉ膜）との間の接着性が著しく低下し、その間で剥離が生じてしまい、電子部品としての必要十分な機械的強度が得られないという欠点がある。すなわち、端子電極のニッケルメッキ膜にリード線を設けた場合、このリード線が容易に剥離してしまう。
【０００８】また、例えば、特開昭５９－２２５５０９号公報に記載されているように、積層セラミックコンデンサに、酸化ルテニウム等の抵抗体ペーストを積層し、これを同時焼成して抵抗体としたものも知られている。しかしながら、これにそのまま端子電極を設けた場合、等価回路がＣ／Ｒまたは（ＬＣ／Ｒ）の並列回路となり、直列回路を得ることができない。また、直列回路を得るためには端子電極の形状が複雑となり、製造工程も複雑なものとなってしまう。
【０００９】なお、酸化物抵抗体の多くは温度依存性を有するものが多く、温度条件が変化する環境で使用する装置等には、温度依存性の小さいデバイスも望まれてい

る。さらに上記の従来のコンデンサの構造では、ＥＳＲの制御が非常に難しく、所望の抵抗値を容易に得ることができない。

【００１０】最近では、電源を含む種々の装置、または電気機器、電子機器が様々な環境下で使用されることから、過酷な使用条件下でも特性の変化のないことが求められている。特にＥＳＲは経時に対して安定していることが重要である。

【００１１】

【発明が解決しようとする課題】この発明の目的は、通常の積層セラミックコンデンサの製造工程を全く変えることなく、容易にＥＳＲを制御でき、かつ信頼性試験においても極めて安定した積層セラミックコンデンサと、そのコンデンサを製造するために適した製造方法とを提供することである。

【００１２】

【課題を解決するための手段】上記目的を達成するために、本発明に係る積層セラミックコンデンサは、内部電極層と誘電体層とが交互に積層された積層セラミックコンデンサにおいて、静電容量に関与しない内部電極層の引き出し部の抵抗が、静電容量に関与する重なり部の抵抗より大きな抵抗を有することを特徴とする。

【００１３】前記引き出し部の抵抗を、重なり部の抵抗より大きくするためには、前記引き出し部の横断面積を、前記重なり部の横断面積よりも小さくすれば良い。

【００１４】前記引き出し部が、線状パターンを含むことが好ましい。

【００１５】前記引き出し部の厚みを、前記重なり部の厚みよりも小さくしても良い。

【００１６】本発明の第１の観点に係る積層セラミックコンデンサの製造方法は、内部電極層と誘電体層とを交互に積層する工程を有する積層セラミックコンデンサの製造方法において、誘電体層の上に内部電極層のパターンを形成する際に、静電容量に関与しない内部電極層の引き出し部の抵抗が、静電容量に関与する重なり部の抵抗より大きな抵抗を有するように、引き出し部のパターン形状を選択することを特徴とする。

【００１７】本発明の第２の観点に係る積層セラミックコンデンサの製造方法は、内部電極層と誘電体層とを交互に積層する工程を有する積層セラミックコンデンサの製造方法において、誘電体層の上に内部電極層のパターンを形成する際に、積層セラミックコンデンサの等価直列抵抗が所定の値となるように、静電容量に関与しない内部電極層の引き出し部のパターン形状を、静電容量に関与する重なり部のパターン形状と異ならせることを特徴とする。

【００１８】

【作用】本発明では、内部電極層における引き出し部のパターンを変える以外は、積層セラミックコンデンサの製造工程を全く変更することなく、ＥＳＲを容易に制御できる積層セラミックコンデンサを製造することができる。

【００１９】積層セラミックコンデンサの内部電極層の形状は、通常、平面側から見て四角形状を成している。これは誘電体層を介して対向する内部電極層との重なり部の面積を大きくし、静電容量を最大限に取得するためである。また、内部電極層の引き出し部は、端子電極との接続を確保するためだけのものであり、静電容量には全く寄与しない。

【００２０】本発明では、特に、この引き出し部のパターン形状または厚みを重なり部のパターン形状に対して変化させることで、コンデンサのＥＳＲを制御することができる。したがって、本発明では、引き出し部の形状または厚みを変えるのみで、静電容量を全く低下させずに、ＥＳＲの制御が可能となる。

【００２１】

【発明の実施の形態】以下、本発明を、図面に示す実施形態に基づき説明する。図１は本発明の一実施形態に係る積層セラミックコンデンサの断面図、図２は図１に示すII－II線に沿う断面図、図３～図５は本発明の他の実施形態に係る内部電極層のパターンを示す断面図、図６（Ａ）は本発明のさらにその他の実施形態に係る内部電極層のパターンを示す平面図、図６（Ｂ）は図６（Ａ）のVIB－VIB線に沿う要部断面図である。

【００２２】第１実施形態

図１に示すように、本発明の一実施形態に係る積層セラミックコンデンサ１は、誘電体層２と内部電極層３とが交互に積層された構成のコンデンサ素子本体１０を有する。このコンデンサ素子本体１０のＸ方向両端部には、素子本体１０の内部で交互に配置された内部電極層３と各々導通する一対の外部端子電極４が形成してある。コンデンサ素子本体１０の形状に特に制限はないが、通常、直方体状とされる。また、その寸法にも特に制限はなく、用途に応じて適当な寸法とすればよいが、通常、（０．６～５．６mm）×（０．３～５．０mm）×（０．３～１．９mm）程度である。

【００２３】各内部電極層３は、図２に示すように、重なり部１２と、重なり部１２に引き出し部１４を介して接続される接続部１６とを有する。図２に示す内部電極層３のパターンの下または上に誘電体層２を介して積層される内部電極層３のパターンは、図２に示す内部電極層３のパターンとＸ方向の左右が逆になる。そして、誘電体層２を介して交互に積層される内部電極層３の接続部１６は、図１に示すコンデンサ素子本体１０の対向する２端部の表面に交互に露出し、それらの部分に配置される一対の外部端子電極４にそれぞれ接続される。その結果、誘電体層２を介して積層された内部電極層３は、コンデンサ回路を構成する。

【００２４】各内部電極層３において、重なり部１２は、誘電体層２を介して交互に積層される内部電極層３

が平面矢視側から見て重なる部分であり、その部分が、コンデンサの静電容量に関与する。また、引き出し部１４および接続部１６は、誘電体層２を介して交互に積層される内部電極層３が平面矢視側から見て重ならない部分であり、コンデンサの静電容量に関与せず、外部端子電極４との接続を図る部分である。

【００２５】重なり部１２は、静電容量に関与する部分であることから、静電容量を向上させるためには、可能な限り大面積であることが好ましく、本実施形態では、平面矢視側から見て矩形状のパターンである。接続部１６は、図１に示す外部端子電極４に直接に接続される部分であり、確実な接続を図るために、重なり部１２と略同程度のＹ方向幅を有することが好ましい。

【００２６】図２に示すように、本実施形態では、静電容量に関与しない内部電極層３の引き出し部１４の抵抗が、静電容量に関与する重なり部１２の抵抗より大きな抵抗を有するように、引き出し部１４のパターンを、Ｘ方向に伸びる線状パターンとしている。本実施形態では、引き出し部１４を構成する線状パターンを２本とし、２本の線状パターンで重なり部１２と接続部１６とを電気的に接続している。引き出し部１４を構成する２本の線状パターンの間には、隙間１５が形成され、その隙間１５では、積層方向の誘電体層２が連続している。引き出し部１４を構成する線状パターンの線幅は、特に限定されないが、最小で、内部電極層３の厚みと同程度であり、最大で、重なり部１２の幅の１／２である。

【００２７】次に本実施形態の積層セラミックコンデンサ１の製造方法を詳細に示す。

［誘電体層用ペースト］誘電体層用ペーストは、誘電体原料と有機ビヒクルとを混練して製造される。誘電体原料には、誘電体層の組成に応じた粉末を用いる。誘電体材料としては特に限定されるものではなく、種々の誘電体材料を用いて良いが、例えば、酸化チタン、チタン系複合酸化物、あるいはこれらの混合物等が好ましい。酸化チタン系としては、必要に応じてＮｉＯ，ＣｕＯ，Mn_3O_4，Al_2O_3，ＭｇＯ，SiO_2等を総計０．００１～３０ｗｔ％程度添加したTiO_2系が挙げられる。また、チタン酸系複合酸化物としては、チタン酸バリウム$BaTiO_3$等が挙げられる。Ｂａ／Ｔｉの原子比は、０．９５～１．２０程度が良く、$BaTiO_3$には、ＭｇＯ，ＣａＯ，Mn_3O_4，Y_2O_3，V_2O_5，ＺｎＯ，ZrO_2，Nb_2O_5，Cr_2O_3，Fe_2O_3，P_2O_5，Na_2O，K_2O等が総計０．００１～３０ｗｔ％程度添加されていても良い。また、焼成温度、線膨張率の調整のため、（Ｂａ，Ｃａ）SiO_2ガラス等のガラスが添加されていても良い。

【００２８】誘電体原料の製造方法は特に限定されず、例えばチタン酸バリウムを用いる場合、水熱合成した$BaTiO_3$に、副成分原料を混合する方法を用いることができる。また$BaCO_3$とTiO_2と副成分原料との混合物を仮焼して固相反応させる乾式合成法を用いても良い。また、共沈法、ゾル・ゲル法、アルカリ加水分解法、沈殿混合法等により得た沈殿物と副成分原料との混合物を仮焼して合成しても良い。なお、副成分には、酸化物や、焼成により酸化物となる各種化合物、例えば、炭酸塩、シュウ酸塩、水酸化物、有機金属化合物等の少なくとも一種以上を用いることができる。誘電体材料の平均粒径は、目的とする誘電体層の平均結晶粒径に応じて決定すれば良いが、通常、平均粒子径０．３～１．０μｍ程度の粉末を用いる。誘電体ペーストは、誘電体原料とを有機ビヒクルとを混練して製造される。

【００２９】有機ビヒクルは、バインダーを有機溶剤中に溶解したものである。有機ビヒクルに用いるバインダーは特に限定されず、エチルセルロース等の通常の各種バインダーから適宜選択すれば良い。また、用いる有機溶剤も特に限定されず、印刷法やシート法、利用する方法に応じて、ターピネオール、ブチルカルビトール、アセトン、トルエン等の各種有機溶剤から適宜選択すれば良い。

【００３０】誘電体層の一層あたりの厚さは特に限定されないが、通常１．５～２０μｍ程度である。また誘電体層の積層数は、通常、１００～３００程度である。

【００３１】［内部電極層用ペースト］内部電極層用ペーストの導電材は特に限定されないが、Ｎｉ，Ｃｕより選ばれる少なくとも一種以上からなることが好ましい。また、誘電体層構成材料に耐還元性を有するものを使用することで、安価な卑金属を用いることができる。このため、導電材としては、特にＮｉあるいはＮｉ合金が好ましい。Ｎｉ合金としては、Ｍｎ，Ｃｒ，Ｃｏ，Ａｌ等から選択される一種以上の元素とＮｉの合金が好ましく、合金中のＮｉ含有量は９５ｗｔ％以上であることが好ましい。なお、ＮｉまたはＮｉ合金中には、Ｐ等の各種微量成分が０．１ｗｔ％程度以下含まれていても良い。

【００３２】内部電極用ペーストは、上記各種導電性金属や合金、あるいは焼成後に上記した導電材となる各種酸化物、有機金属化合物、レジネート等と上記した有機ビヒクルとを混練して調整する。内部電極層３の厚さは用途に応じて、適宜決定すれば良いが、０．５～５μｍ程度であることが好ましい。

【００３３】［外部端子電極用ペースト］外部端子電極用ペーストは、導電材とガラスフリットと有機ビヒクルとを含む。前記導電材は、Ａｇ，Ａｕ，Ｐｔ，Ｐｄ，Ｃｕ，Ｎｉから少なくとも一種以上から選ばれるが、安価であることからＣｕ，Ｎｉ、あるいはそれら合金が好ましく、特にＣｕが好ましい。これら導電材に、焼結助剤、あるいはチップ素体との接着を確保するためにガラスフリットが添加される。

【００３４】導電材の平均粒径は０．０１～１０μｍとする。これよりも粒径が小さい場合、導電材粒子の凝集が激しくなり、端子電極用ペーストの塗布、乾燥時に、あるいは焼き付け時に、端子電極にクラックが生じやすくなり、これよりも粒径が大きい場合、ペースト化が困難になる。また、ガラスフリットの平均粒径は０．０１～３０μｍとする。これよりも粒径が小さいと導電材の焼結が不均一となり、端子電極にクラックを発生させる原因となり、これよりも大きいと、ガラスの分散が悪くなり、端子電極と素体との接着性が低下する傾向にある。これら導電材およびガラスフリットをビヒクル中に分散して端子電極用ペーストを得る。

【００３５】ガラスフリット組成は、特に限定されるものではない。ただし導電材にＣｕを用いた場合は中性、あるいは還元性雰囲気で端子電極を焼成する必要上、それら雰囲気下でもガラスとしての機能を果たすものであることが必要である。このようなものとしては、例えば、ケイ酸ガラス（SiO_2　：２０～８０ｗｔ％，Na_2O：８０～２０ｗｔ％）、ホウケイ酸ガラス（B_2O_3　：５～５０ｗｔ％，SiO_2　：５～７０ｗｔ％，ＰｂＯ：１～１０ｗｔ％，K_2O：１～１５ｗｔ％）、アルミナケイ酸ガラス（Al_2O_3　：１～３０ｗｔ％，SiO_2　：１０～６０ｗｔ％，Na_2O：５～１５ｗｔ％，ＣａＯ：１～２０ｗｔ％，B_2O_3　：５～３０ｗｔ％）から選択されるガラスフリットの一種または二種以上を用いれば良い。これに必要に応じて、ＣａＯ：０．０１～５０ｗｔ％，ＢａＯ：０．０１～５０ｗｔ％，ＭｇＯ：０．０１～５ｗｔ％，～ＺｎＯ：０．０１～７０ｗｔ％，ＰｂＯ：０．０１～５ｗｔ％，Na_2O：０．０１～１０ｗｔ％，K_2O：０．０１～１０ｗｔ％，MnO_2　：０．０１～２０ｗｔ％等の添加物を所定の組成になるように混合して用いれば良い。導電材である金属成分に対するガラスの含有量は特に限定されるものではないが、通常、金属成分に対して０．５～１５ｗｔ％程度である。有機ビヒクルとしては上述のものを用いれば良い。

【００３６】［有機ビヒクルの含有量］上記した各ペースト中の有機ビヒクルの含有量に特に制限はなく、通常の含有量、例えばバインダーは１～５ｗｔ％程度、溶剤は１０～５０ｗｔ％とすれば良い。また、各ペースト中には、必要に応じて各種分散剤、可塑剤、誘電体、絶縁体等から選択される添加剤が含有されていても良い。これらの総含有量は、１０ｗｔ％以下とすることが好ましい。

【００３７】［グリーンチップの作製］印刷法を用いる場合、誘電体用ペーストおよび内部電極用ペーストをＰＥＴ等の基板状に印刷する。このとき内部電極用ペーストの端部の一方が誘電体ペーストの端部より交互に外部に露出するように積層する。その後、熱圧着し、所定形状に切断してチップ化した後、基板から剥離してグリーンチップとする。

【００３８】また、シート法を用いる場合、誘電体層用ペーストを用いてグリーンシートを形成し、このグリーンシート上に内部電極層用ペーストを印刷し、これらを交互に繰り返して積層し、所定形状に切断してグリーンチップとする。

【００３９】本実施形態では、内部電極用ペーストを印刷する際に、たとえば図２に示すように、重なり部１２、引き出し部１４および接続部１６から成る内部電極用パターンを形成する。

【００４０】［脱バインダー工程］焼成前に行う脱バインダー処理の条件は、通常のものであっても良いが、内部電極層の導電材にＮｉやＮｉ合金等の卑金属を用いる場合、特に下記の条件で行うことが好ましい。

昇温速度：５～３００℃／時間、特に１０～１００℃／時間

保持温度：２００～４００℃／時間、特に２５０～３００℃／時間

温度保持時間：０．５～２４時間、特に５～２０時間

雰囲気：空気中

［焼成工程］グリーンチップの焼成時の雰囲気は、内部電極用ペーストの導電材の種類に応じて適宜選択すれば良いが、導電材としてＮｉやＮｉ合金等の卑金属を用いる場合、焼成雰囲気はN_2　を主成分とし、H_2　を１～１０％、１０～３５℃における水蒸気圧によって得られるH_2　Ｏガスを混合したものが好ましい。酸素分圧は10^{-8}～10^{-12}　気圧とすることが好ましい。酸素分圧が前記範囲未満であると、内部電極の導電材が異常焼結を起こし、途切れてしまうことがある。また、酸素分圧が前記範囲を越えると、内部電極が酸化してしまう傾向にある。焼成時の保持温度は、１１００～１４００℃、特に１２００～１３００℃とすることが好ましい。保持温度が前記範囲未満であると緻密化が不十分であり、前記範囲を越えると、内部電極が途切れやすくなる。また、焼成時の温度保持時間は、０．５～８時間、特に１～３時間が好ましい。

【００４１】［アニール工程］還元雰囲気で焼成した場合、積層チップコンデンサにはアニールを施すことが好ましい。アニールは、誘電体層を再酸化するための処理であり、これにより絶縁抵抗の加速寿命を著しく長くすることができる。

【００４２】アニール雰囲気の酸素分圧は、10^{-6}気圧以上、特に10^{-6}～10^{-8}気圧とすることが好ましい。酸素分圧が前記範囲未満であると誘電体層の再酸化が困難であり、前記範囲を越えると内部電極が酸化する。

【００４３】アニールの保持温度は、１１００℃以下、特に５００～１０００℃とすることが好ましい。保持温度が前記範囲未満であると、誘電体層の酸化が不十分となり、絶縁抵抗の加速寿命が短くなる傾向を示し、前記

範囲を越えると内部電極が酸化し、容量が低下するだけでなく、誘電体素地と反応し、加速寿命も短くなる。なお、アニール工程は昇温および降温だけから構成しても良い。この場合、温度保持時間をとる必要なく、保持温度は最高温度と同義である。また、温度保持時間は、０～２０時間、特に２～１０時間が好ましい。雰囲気ガスには、N_2 と加湿したH_2 ガスを用いることが好ましい。

【００４４】なお、上記した脱バインダー処理、焼成およびアニールの各工程において、N_2 ，H_2 や混合ガス等を加湿するには、例えば、ウエッター等を使用すれば良い。この場合の水温は、５～７５℃程度が好ましい。脱バインダー処理工程、焼成工程およびアニール工程は、連続して行っても、独立して行っても良い。これらを連続して行う場合、脱バインダー処理後、冷却せず雰囲気を変更、独立して行っても良い。これらを連続して行う場合、脱バインダー処理後、冷却せず雰囲気を変更し、続いて焼成の保持温度まで昇温して焼成を行い、ついで冷却し、アニール工程での保持温度に達したときに雰囲気を変更してアニールを行うことが好ましい。

【００４５】また、これらを独立して行う場合は、脱バインダー処理工程は、所定の保持温度まで昇温し、所定時間保持した後、室温まで降温する。その際の脱バインダー雰囲気は連続して行う場合と同様なものとする。また脱バインダー工程と焼成工程とを連続して行い、アニール工程だけを独立して行うようにしても良く、脱バインダー工程だけを独立して行い、焼成工程とアニール工程を連続して行うようにしても良い。

【００４６】［端子電極形成］端子電極用ペーストを焼結体チップに塗布する。塗布工程としては特に限定されるものではないが、ディップ法等によれば良い。端子電極用ペーストの塗布量は、特に限定されるものではなく、塗布する焼結体チップの大きさなどにより適宜調整すれば良いが、通常、５～１００μｍ程度である。端子電極用ペーストを塗布後、乾燥する。乾燥は６０～１５０℃程度で、１０分～１時間程度行うことが好ましい。

【００４７】上記のようにして端子電極用ペーストを塗布、乾燥した後、チップ素体への焼き付けを行う。焼き付け条件は、例えば、N_2 の中性雰囲気、あるいはN_2とH_2 との混合ガス等の還元雰囲気中にて６００℃～１０００℃で０～１時間程度保持することにより行うことが好ましい。

【００４８】［メッキ層］必要に応じて上記端子電極上にＮｉ層とＳｎ層またはＳｎ－Ｐｂ合金層を電解メッキ法にて形成する。メッキ層の厚みは特に限定されないが、通常、０．１～１０μｍ程度である。

【００４９】［積層セラミックコンデンサおよびその製造方法の作用］本実施形態では、内部電極層３における引き出し部１４のパターンを変える以外は、積層セラミックコンデンサの製造工程を全く変更することなく、ＥＳＲを容易に制御できる積層セラミックコンデンサ１を製造することができる。

【００５０】本実施形態では、特に、この引き出し部１４のパターン形状を重なり部１２のパターン形状に対して変化させることで、コンデンサのＥＳＲを制御することができる。したがって、本実施形態では、引き出し部１４の形状を変えるのみで、静電容量を全く低下させずに、ＥＳＲの制御が可能となる。

【００５１】ＥＳＲの具体的な値は、特に限定されるものではないが、通常、０．５Ω～１０Ω程度であり、好ましくは０．５～５Ωである。この範囲のＥＳＲを有する積層セラミックコンデンサは、レギュレータＩＣ用のコンデンサとして十分な性能を発揮することができる。

【００５２】第２実施形態

図３に示すように、本実施形態に係る積層セラミックコンデンサ１ａでは、誘電体層２を介して積層される内部電極層３ａの重なり部１２ａおよび接続部１６ａのパターン形状は、図２に示す実施形態のものと同様とし、引き出し部１４ａのパターン形状のみを、図２に示す実施形態のものと相違させている。

【００５３】すなわち、本実施形態では、引き出し部１４ａを、Ｘ方向に伸びる４本の線状パターンで構成してあり、これら線状パターンにより重なり部１２ａと接続部１６ａとを接続している。引き出し部１４ａを構成する線状パターンの本数を制御することで、最終的に得られる積層セラミックコンデンサのＥＳＲを制御することができる。線状パターンの本数が多くなるほど、引き出し部１４ａの抵抗が低下する。本実施形態に係る積層セラミックコンデンサ１ａでも、前記第１実施形態に係る積層セラミックコンデンサ１と同様な作用を奏する。

【００５４】第３実施形態

図４に示すように、本実施形態に係る積層セラミックコンデンサ１ｂでは、誘電体層２を介して積層される内部電極層３ｂの重なり部１２ｂおよび接続部１６ｂのパターン形状は、図２に示す実施形態のものと同様とし、引き出し部１４ｂのパターン形状のみを、図２に示す実施形態のものと相違させている。

【００５５】すなわち、本実施形態では、引き出し部１４ｂを、Ｘ方向に伸びる５本の線状パターンと、これらの中間位置を結ぶようにＹ方向に伸びる線状パターン１８ｂとで構成してあり、これら線状パターンにより重なり部１２ｂと接続部１６ｂとを接続している。引き出し部１４ｂを構成する線状パターンの本数を制御することで、最終的に得られる積層セラミックコンデンサのＥＳＲを制御することができる。線状パターンの本数が多くなるほど、引き出し部１４ｂの抵抗が低下する。　本実施形態に係る積層セラミックコンデンサ１ｂでも、前記第１実施形態に係る積層セラミックコンデンサ１と同様な作用を奏する。

【００５６】第４実施形態

図５に示すように、本実施形態に係る積層セラミックコンデンサ１ｃでは、誘電体層２を介して積層される内部電極層３ｃの重なり部１２ｃのパターン形状は、図２に示す実施形態のものと同様とし、引き出し部１４ｃのパターン形状を、図２に示す実施形態のものと相違させると共に、接続部１６ｃのＸ方向幅を大きくしてある。

【００５７】本実施形態では、引き出し部１４ｃを、Ｘ方向に伸びる５本の線状パターンで構成してあり、これら線状パターンにより重なり部１２ｃと接続部１６ｃとを接続している。引き出し部１４ｃを構成する線状パターンの本数を制御することで、最終的に得られる積層セラミックコンデンサのＥＳＲを制御することができる。線状パターンの本数が多くなるほど、引き出し部１４ｃの抵抗が低下する。本実施形態に係る積層セラミックコンデンサ１ｃでも、前記第１実施形態に係る積層セラミックコンデンサ１と同様な作用を奏する。

【００５８】第５実施形態

図６（Ａ）および（Ｂ）に示すように、本実施形態に係る積層セラミックコンデンサ１ｄでは、誘電体層２を介して積層される内部電極層３ｄの重なり部１２ｄ、引き出し部１４ｄおよび接続部１６ｄの平面矢視パターン形状は、従来のものと同様であるが、引き出し部１４ｄの厚みを、重なり部１２ｄの厚みに比べて薄くしてある点が、従来と異なる。

【００５９】すなわち、本実施形態では、引き出し部１４ｄの厚みを、重なり部１２ｄおよび接続部１６ｄの厚みに比べて薄くしてある。引き出し部１４ｄの厚みを薄くすることで、その部分の抵抗を上げることができる。また、引き出し部１４ｄの厚みを制御することで、最終的に得られる積層セラミックコンデンサのＥＳＲを制御することができる。引き出し部１４ｄの厚みが薄くなるほど、引き出し部１４ｄの抵抗が増大する。本実施形態に係る積層セラミックコンデンサ１ｄでも、前記第１実施形態に係る積層セラミックコンデンサ１と同様な作用を奏する。

【００６０】その他の実施形態

なお、本発明は、上述した実施形態に限定されるものではなく、本発明の範囲内で種々に改変することができる。たとえば、引き出し部１４、１４ａ～１４ｄの形状を変更するパターンは、上述した実施形態に限定されるものではなく、引き出し部のパターンが螺旋状パターンであっても、波状パターンであっても良く、また他のいかなるパターン形状であってもかまわない。

【００６１】さらに、本発明では、内部電極層の引き出し部１４、１４ａ～１４ｄを、重なり部１２、１２ａ～１２ｄよりも抵抗の高い導電材で構成することによっても同様な作用効果が得られる。

【００６２】

【実施例】以下、本発明を、さらに詳細な実施例に基づき説明するが、本発明は、これら実施例に限定されない。

【００６３】実施例１

誘電体層の主原料として$BaCO_3$（平均粒径：２．０μｍ）およびTiO_2（平均粒径：２．０μｍ）を用意した。Ｂａ／Ｔｉの原子比は１．００である。また、これに加えて、$BaTiO_3$に対し、添加物として$MnCO_3$を０．２ｗｔ％、$MgCO_3$を０．２ｗｔ％、Y_2O_3を２．１ｗｔ％、（Ｂａ，Ｃａ）SiO_3を２．２ｗｔ％用意した。各原料粉末を水中ボールミルで混合し、乾燥した。得られた混合粉を１２５０℃で２時間仮焼した。この仮焼粉を水中ボールミルで粉砕し、乾燥した。得られた仮焼粉に、有機バインダーとしてアクリル樹脂と有機溶剤として塩化メチレンとアセトンを加えてさらに混合し、誘電体スラリーとした。得られた誘電体スラリーをドクターブレード法にて誘電体グリーンシートとした。

【００６４】内部電極層材料としてＮｉ粉末（平均粒径：０．８μｍ）を用意し、これに有機バインダーとしてエチルセルロースと、有機溶剤としてターピネオールを加え、三本ロールを用いて混練し、内部電極ペーストとした。

【００６５】外部端子電極の導電材料として、Ｃｕ粉末（平均粒径：０．５μｍ）とＣｕ粉末に対してストロンチウム系ガラスフリットを７ｗｔ％添加し、これに有機バインダーとしてアクリル樹脂と有機溶剤としてターピネオールを加え、三本ロールを用いて混練し、第１金属層用ペーストとした。

【００６６】所定の厚みを得るために誘電体グリーンシートを数枚積層し、その上にスクリーン印刷法により、図２に示した内部電極パターンを用いて、内部電極用ペーストの端部が誘電体層用グリーンシートの端部から交互に外部に露出するように印刷されたグリーンシートを２００枚積層し、熱圧着した。次いで、焼成後のチップ形状が、縦２．０×横１．２×厚み１．２mmになるように切断し、グリーンチップを得た。

【００６７】得られたグリーンチップを、加湿したN_2+H_2（H_2：３％）雰囲気中、１３００℃にて３時間保持して焼成し、さらに加湿したH_2酸素分圧10^{-7}気圧の雰囲気にて１０００℃で２時間保持し、チップ焼結体を得た。得られた焼結体の両端部に上記端子電極用ペーストを塗布し、その後に乾燥し、N_2-H_2雰囲気中、７７０℃で１０分間保持して熱処理を行い、端子電極を得た。

【００６８】その後、該端子電極上にＮｉ，Ｓｎの順に電解メッキ法にてメッキ膜を形成した。得られた積層セラミックコンデンサ試料の静電容量は２．０μＦであった。

【００６９】図１に示す内部電極構造を積層して作製した積層セラミックコンデンサの静電容量とＥＳＲの値を表１に示す。測定した個数は５０個であり、その平均値

を示す。ＥＳＲは、ＬＣＲメータにより測定した。

【００７０】

【表１】

内部電極パターンと電気特性

	静電容量（μＦ）	ＥＳＲ（Ω）
実施例１	２．０	２．４４
実施例２	２．０	１．１０
実施例３	２．０	０．９２
実施例４	２．０	０．６８
比較例１	２．０	０．０００５

【００７１】また、本実施例１の積層セラミックコンデンサを、レギュレータＩＣの平滑用コンデンサとして用い１００ｋＨｚで動作させたところ、発振等の電圧変動を生じることなく正常に動作した。

【００７２】また、コンデンサの加速試験である高温負荷試験（８５℃、定格の２倍の電圧印加、１０００時間）および耐湿負荷試験（８５℃、８５％、定格電圧印加、１０００時間）でもＥＳＲの変動およびその他の電気特性（静電容量、絶縁抵抗）に変化は認められなかった。

【００７３】実施例２

内部電極層のパターンとして、図３に示すパターンとした以外は、前記実施例１と同様にして、積層セラミックコンデンサ試料を作製し、静電容量とＥＳＲの値を求めた。結果を表１に示す。

【００７４】また、本実施例２の積層セラミックコンデンサを、レギュレータＩＣの平滑用コンデンサとして用い１００ｋＨｚで動作させたところ、発振等の電圧変動を生じることなく正常に動作した。

【００７５】また、コンデンサの加速試験である高温負荷試験および耐湿負荷試験でもＥＳＲの変動およびその他の電気特性（静電容量、絶縁抵抗）に変化は認められなかった。

【００７６】実施例３

内部電極層のパターンとして、図４に示すパターンとした以外は、前記実施例１と同様にして、積層セラミックコンデンサ試料を作製し、静電容量とＥＳＲの値を求めた。結果を表１に示す。

【００７７】また、本実施例３の積層セラミックコンデンサを、レギュレータＩＣの平滑用コンデンサとして用い１００ｋＨｚで動作させたところ、発振等の電圧変動を生じることなく正常に動作した。

【００７８】また、コンデンサの加速試験である高温負荷試験および耐湿負荷試験でもＥＳＲの変動およびその他の電気特性（静電容量、絶縁抵抗）に変化は認められなかった。

【００７９】実施例４

内部電極層のパターンとして、図５に示すパターンとした以外は、前記実施例１と同様にして、積層セラミックコンデンサ試料を作製し、静電容量とＥＳＲの値を求めた。結果を表１に示す。

【００８０】また、本実施例４の積層セラミックコンデンサを、レギュレータＩＣの平滑用コンデンサとして用い１００ｋＨｚで動作させたところ、発振等の電圧変動を生じることなく正常に動作した。

【００８１】また、コンデンサの加速試験である高温負荷試験および耐湿負荷試験でもＥＳＲの変動およびその他の電気特性（静電容量、絶縁抵抗）に変化は認められなかった。

【００８２】比較例１

内部電極層のパターンとして、重なり部、引き出し部および接続部のパターンが、平面矢視側から見て全て一体的に矩形状となる従来例のパターンとした以外は、前記実施例１と同様にして、積層セラミックコンデンサ試料を作製し、静電容量とＥＳＲの値を求めた。結果を表１に示す。

【００８３】また、比較例１の積層セラミックコンデンサを、レギュレータＩＣの平滑用コンデンサとして用い１００ｋＨｚで動作させたところ、発振等の電圧変動が観察された。

【００８４】また、コンデンサの加速試験である高温負荷試験および耐湿負荷試験において、ＥＳＲの変動が観察された。

【００８５】評価

表１から明らかなように、内部電極の引き出し部の形状、すなわち断面積（または体積）を変えることにより、ＥＳＲを制御できることが分かる。

【００８６】

【発明の効果】以上説明してきたように、本発明によれば、内部電極の引き出し部の形状を選定することにより、容易にＥＳＲの制御が可能となり、内部電極を形成する際のパターンを変更するだけで、通常の積層セラミックコンデンサの工程をほとんど変更せずに、所望のＥＳＲを具備した積層セラミックコンデンサが得られる。

【図面の簡単な説明】

【図１】　図１は本発明の一実施形態に係る積層セラミックコンデンサの断面図である。

【図２】　図２は図１に示すII－II線に沿う断面図である。

【図３】　図３は本発明の他の実施形態に係る内部電極

層のパターンを示す断面図である。

【図４】　図４は本発明のさらに他の実施形態に係る内部電極層のパターンを示す断面図である。

【図５】　図５は本発明のさらに他の実施形態に係る内部電極層のパターンを示す断面図である。

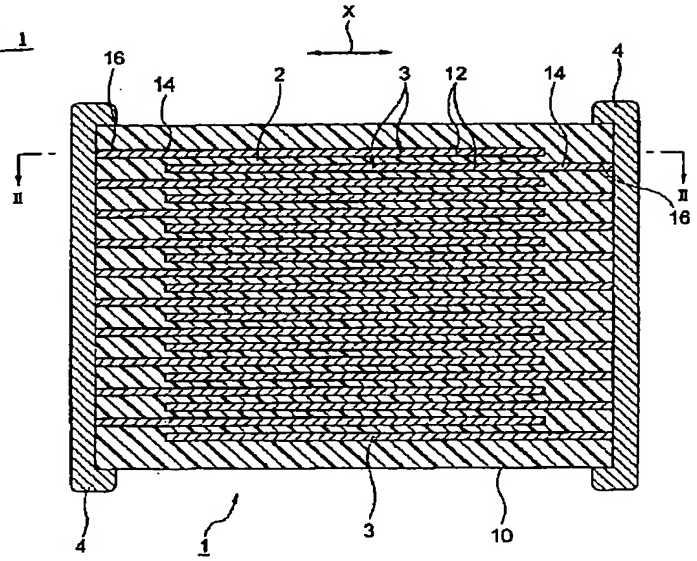
【図６】　図６（Ａ）は本発明のさらにその他の実施形態に係る内部電極層のパターンを示す平面図、図６（Ｂ）は図６（Ａ）のVIB－VIB線に沿う要部断面図である。

【符号の説明】

１，１ａ～１ｄ…　積層セラミックコンデンサ
２…　誘電体層
３…　内部電極層
４…　外部端子電極
１０…　コンデンサ素子素体
１２，１２ａ～１２ｄ…　重なり部
１４，１４ａ～１４ｄ…　引き出し部
１６，１６ａ～１６ｄ…　接続部

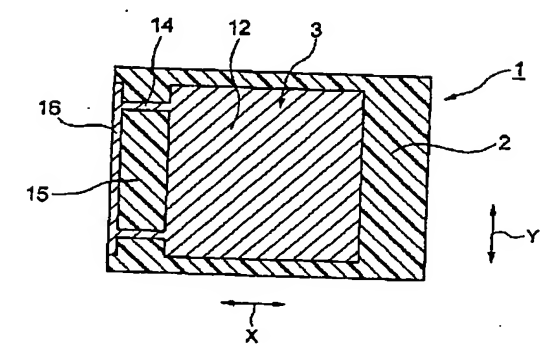
【図１】

図　1



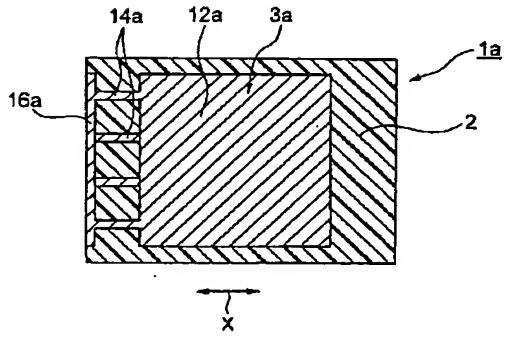
【図２】

図　2



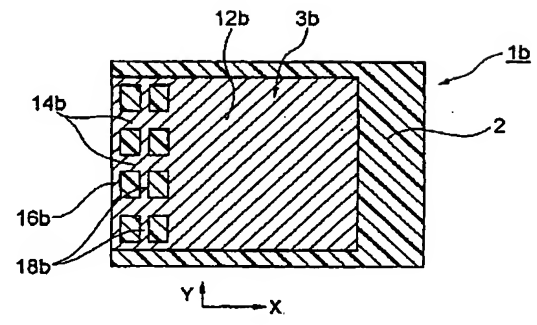
【図３】

図　3.



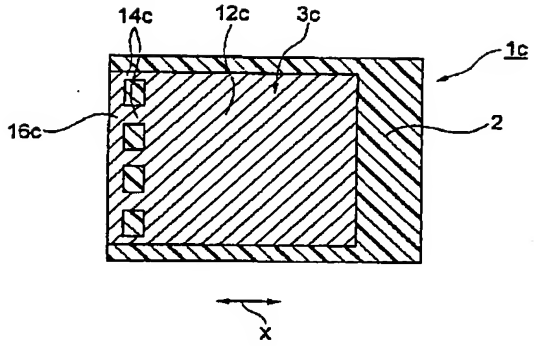
【図４】

図　4



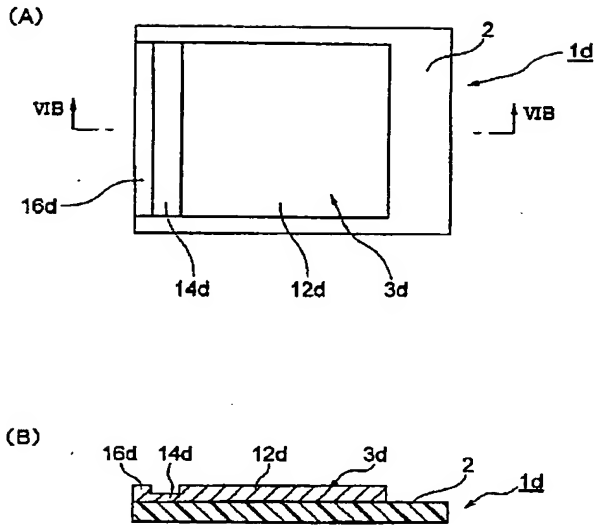
【図５】

図　5



【図６】

図　6



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AH09 AJ01
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EE16 EE23 EE26 EE35 FG06
FG22 FG26 FG27 FG46 FG54
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